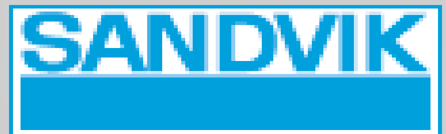


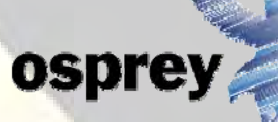


# Performance and Cost Benefits of Si-Al Substrates in the Manufacture of RF and Microwave III-V Semiconductor Devices

Dr. Andrew Ogilvy, Sandvik Osprey Ltd.

Presented by Stu Weinshanker
Advanced Packaging Associates, Inc.

**Microwave and RF Advanced Technology Workshop**
**San Diego, CA**
**September 23, 2009**

International Microelectronics And Packaging Society

and the Microelectronics Foundation

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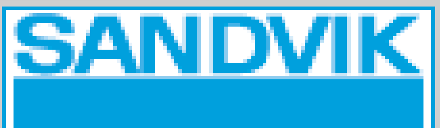

# Overview

# Sandvik Osprey CE Alloys

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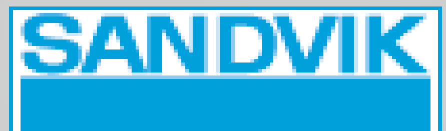


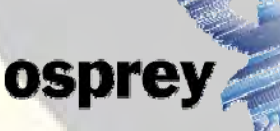


# Sandvik Osprey CE Alloys

## High Performance Microelectronic Packaging Solutions

**Cost Effective, Lightweight, Thermally Enhanced, Mechanically Stable**

***Custom Components, Hermetic Packages***

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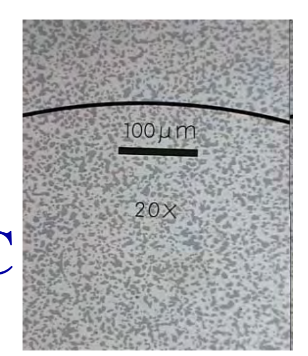
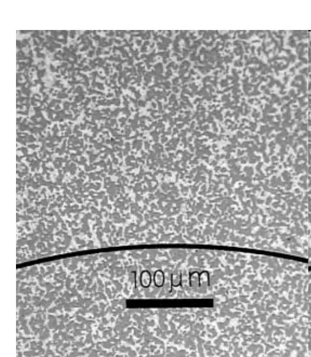
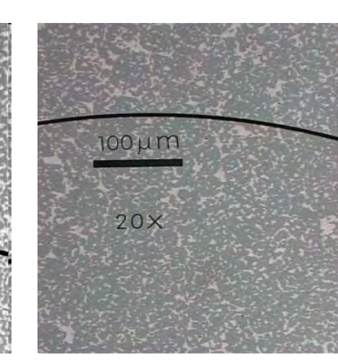
# Osprey CE Alloys - Alloy Range

- Series of binary Silicon Aluminum alloys
- Customers can "dial-in" the required CTE between 17ppm/°C and 5ppm/°C

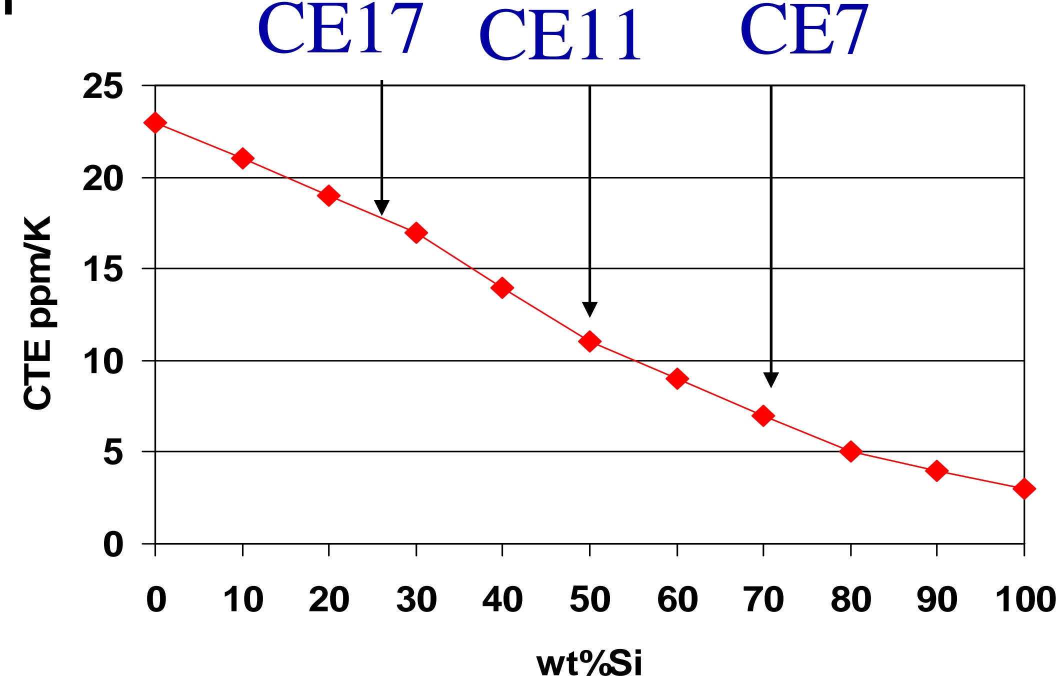
- CE17 Al-27%Si
- CE17M Al-27SiFeMgMn
- CE15 Al-35%Si
- CE13 Al-42%Si
- CE13M Al-27SiFeMgMn
- CE11 Si-50%Al
- CE9 Si-40%Al
- CE7 Si-30%Al
- CE6 Si-20%Al
- CE5 Si-13%Al




CE17 CE11 CE7

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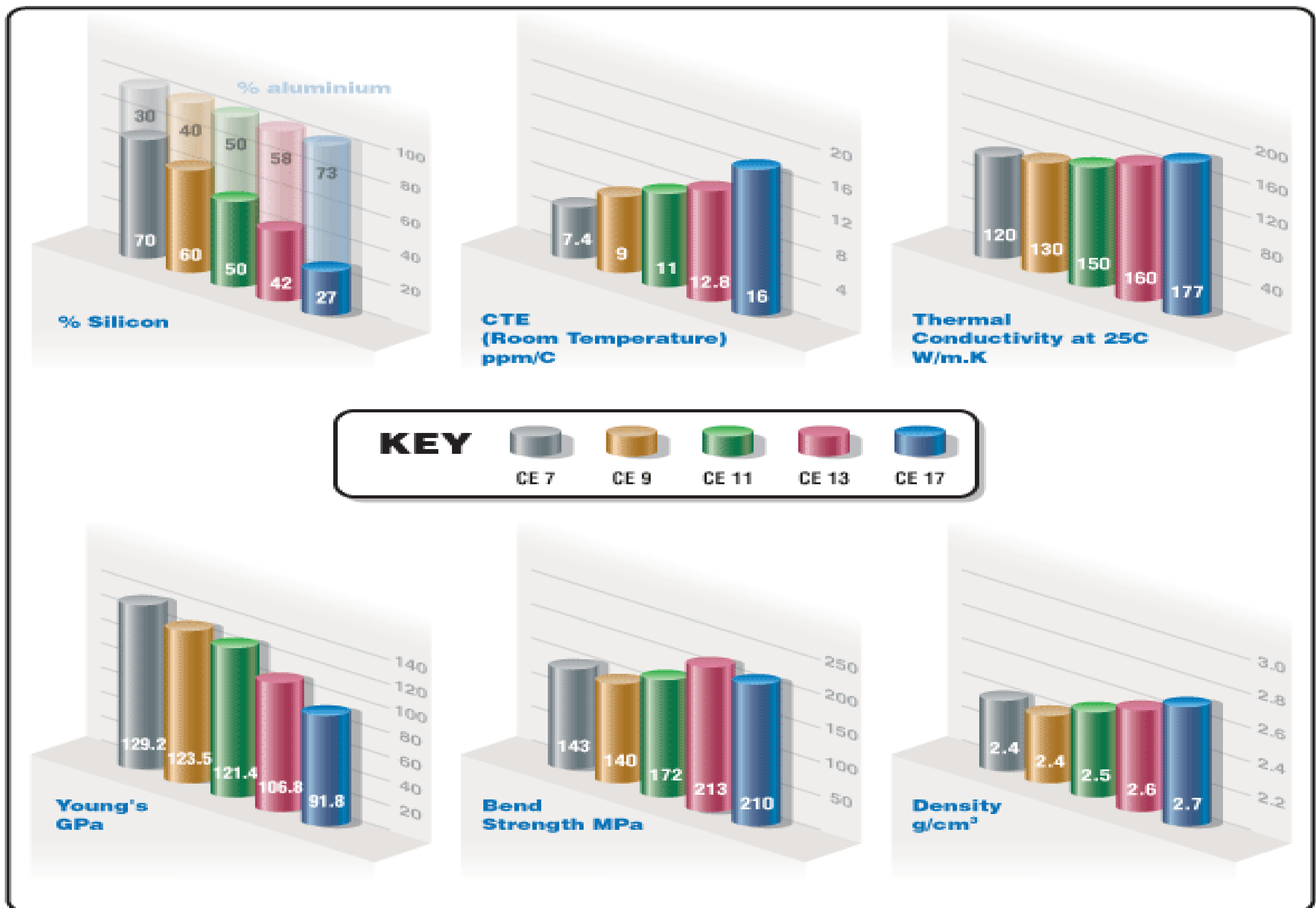


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# Thermal Expansion at Lower Temperatures

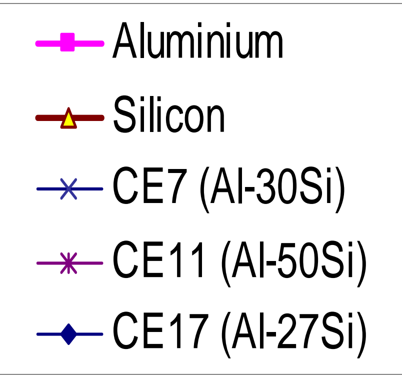
Osprey CE alloys between -100°C and 127°C

CTE, ppm/°C

25
20
15
10
5
0

-100 -50 0 50 100 150

Temperature, °C

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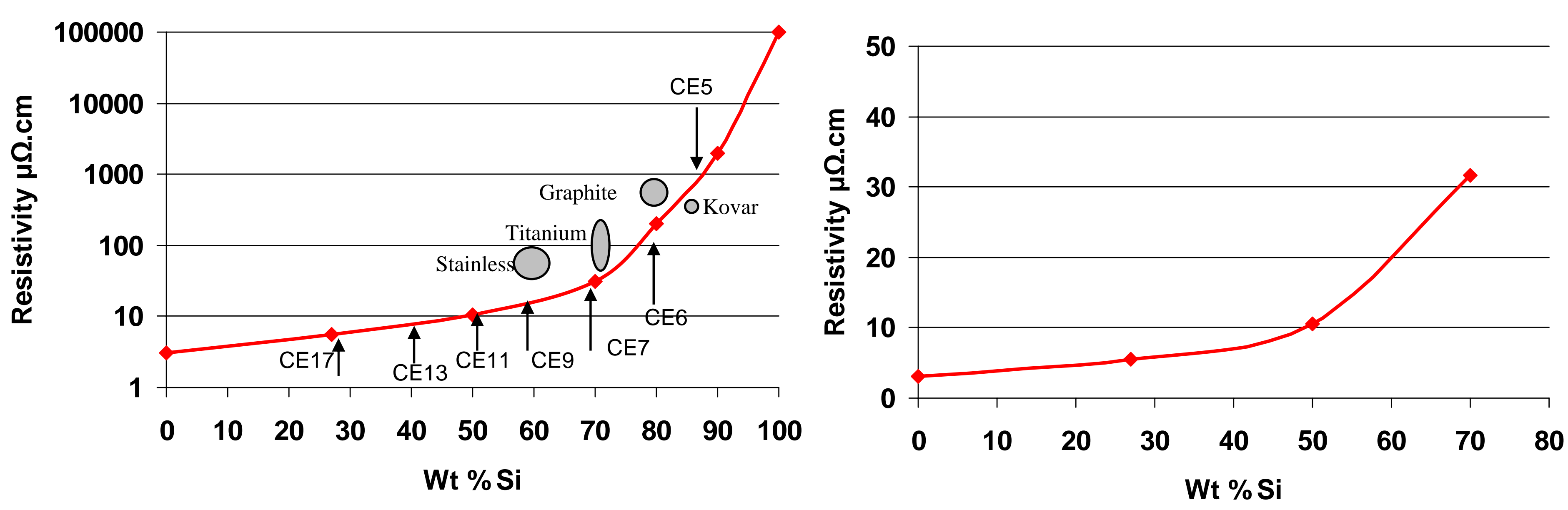
# Resistivity




The CE Alloys are metallic (true binary alloys) and are good electrical conductors up to 80% Si (CE6)

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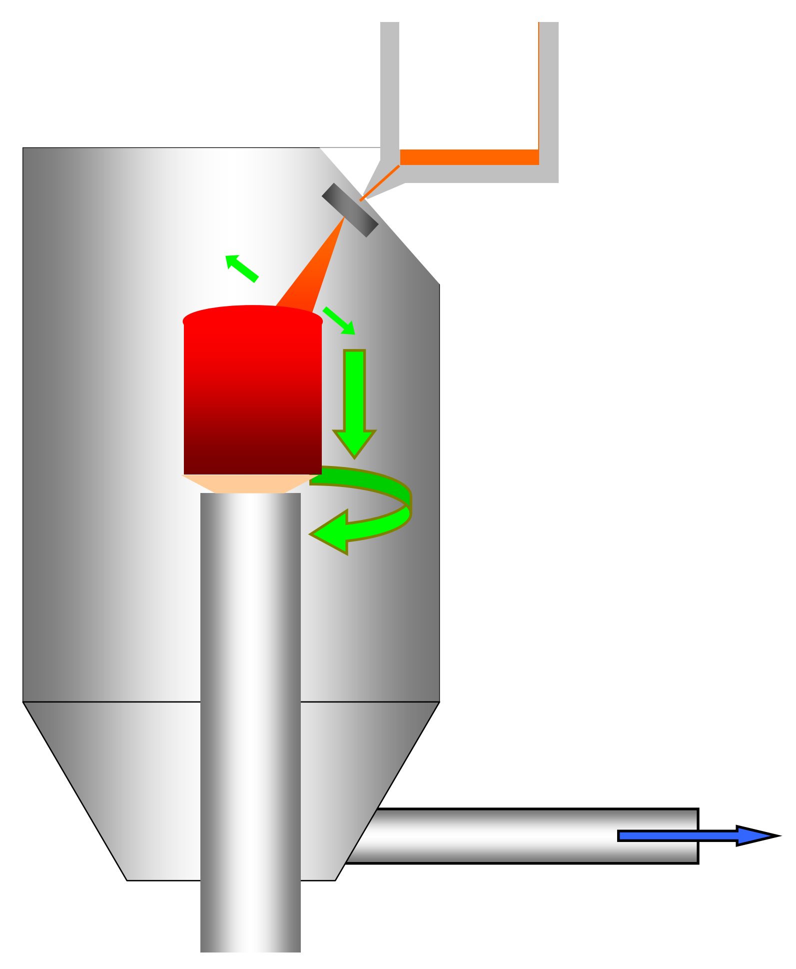
# Spray Forming of the CE Alloys

- Inert gas atomization of molten alloy
- Rapid solidification → fine structure
- Homogeneous, isotropic
- Billets are hipped to full density, verified, fabricated to specification



The Patented Osprey Process

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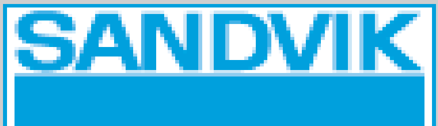

# Introducing

# Sandvik Osprey CE Alloy Wafers

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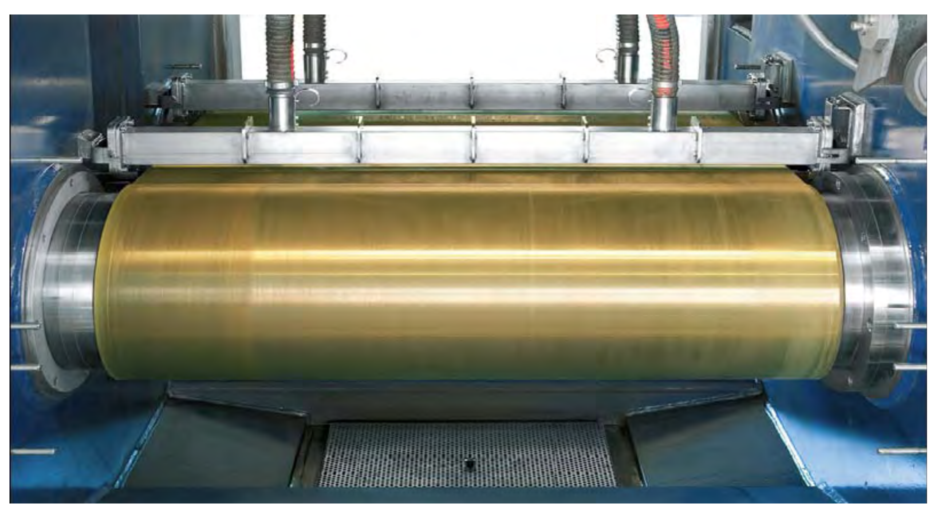
# Wafer Production Route

- CE Alloy Billet is cut and turned to the required diameter, orientation flat(s)
- Wire slurry saw slicing (Ra ~ 0.4micron)
- Lap to thickness (TTV < 5micron)
- Optional polish (Ra <0.02micron)



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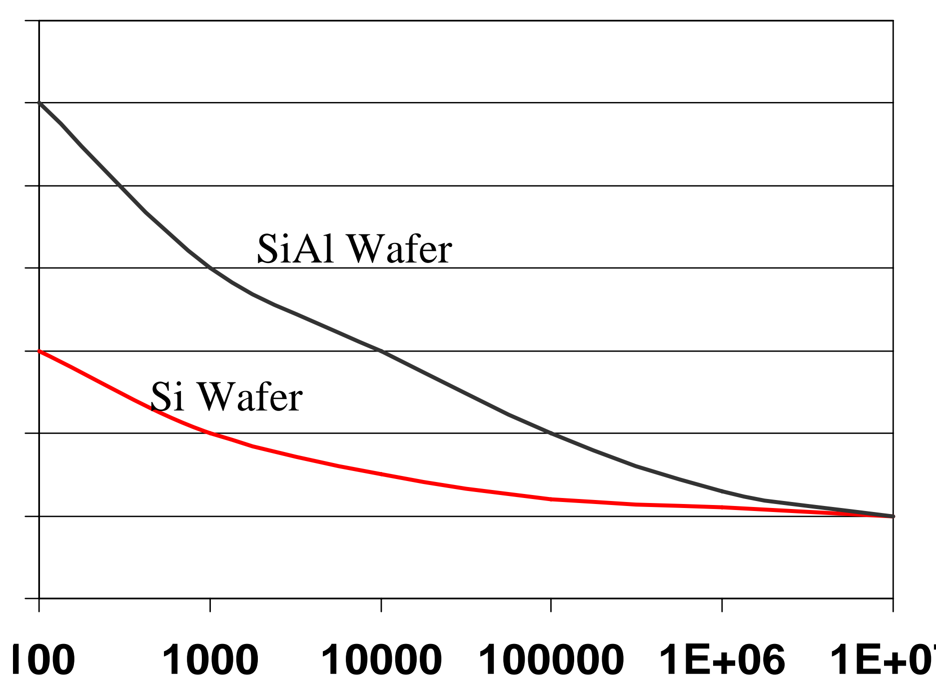
# CE Alloy Volume Wafer Cost

## CE Alloys offer some significant economies of scale

- Comprised of standard purity aluminum and metallurgical grade silicon
  - both extremely common, available
- Spray Formed polycrystalline ingots have lower fab cost than single crystal Si
- Majority of wafer cost is slicing, lapping and polishing, which follow existing, established Si methods.

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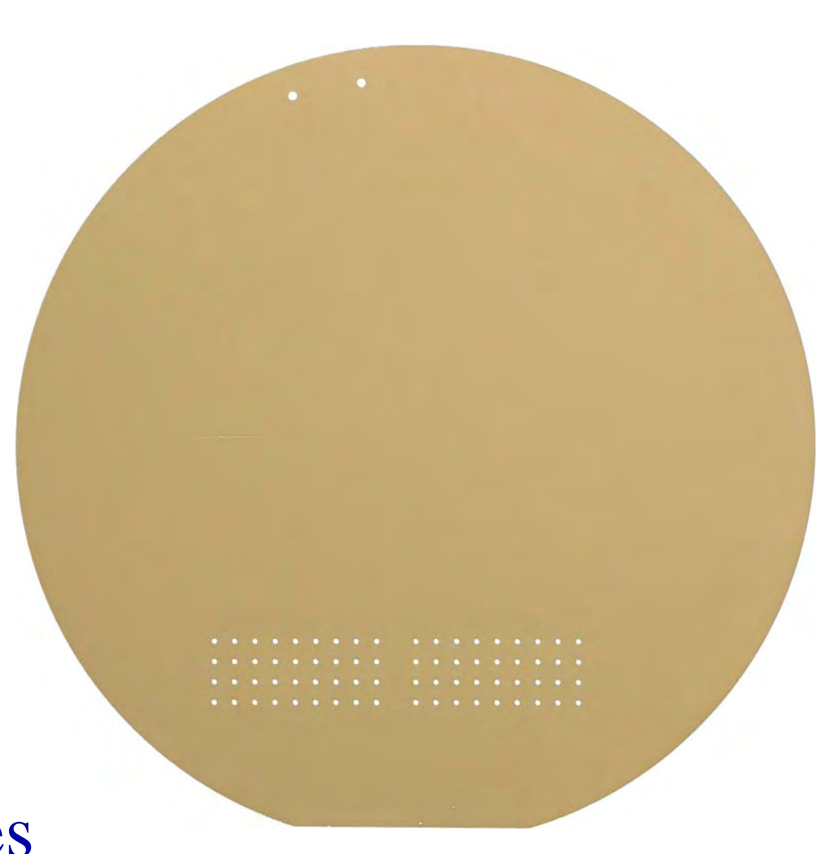
# CE Alloy Wafers

- Wide range of CTE
  - 5 to 17 ppm/deg C
- Up to 12” diameter
- As-cut thickness down to 0.008”
  - Suitable for Back grinding
- Lapped, polished surfaces
- Standard Al coating technology
  - CVD, PVD, Electroplating
  - Options include AuSn solder plating, electrically insulating films
- Cost effective options for thru holes
  - As small as 25 micron diameter



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# Typical CE Alloy Wafer Tolerances

- **Dimensional**
  - Up to 300mm (12”) diameter
  - Diameter tolerance +/-0.05mm
- **Thickness**
  - Down to 0.2 mm +/- 0.02mm (8 mil)
- **TTV**
  - Normally <10 microns on 100mm (4”) wafers
- **Bow and Warp**
  - < 20 micron Bow and Warp on 100mm wafers
- **Surface Finish**
  - standard lapped finish Ra = 0.4 micron.
  - can be polished to Ra = 0.02 micron

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# CE6 alloy developed to match III/V Compound Semiconductors

## Expansion of CE alloys, Sapphire and GaAs

## Normalised to 25°C to 200°C

dL/Lo x $10^{-3}$

1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

0 50 100 150 200

Temp °C

Sapphire
CE6
CE7
CE5
GaAs

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# Wafer Scale Processing, Packaging of III-V Semiconductor Devices Carrier Material Options

| **Property** | **Ge** | **Si** | **GaAs** | **Sapphire** | **CE6** |
|---|---|---|---|---|---|
| CTE 25 – 300°C | 5.8 | 3 | 6.8 | 5.8 | 6.2 |
| Density g/cc | 5.32 | 2.3 | 5.3 | 4.0 | 2.45 |
| Young's Modulus GPa | 130 | 112 | 85 | 350 | 130 |
| Thermal Conductivity W/mK | 64 | 150 | 40 | 35 | 110 |
| Electrical Resistivity μ Ω.cm | 50 | $10^5$ | $10^7$ | $10^{14}$ | 115 |
| Platability | Good | Poor | Poor | Poor | Good |
| Machinability (CNC/.EDM) | Poor | Poor | Poor | Poor | Good |
| Price (cf 4" Si wafer) | 18 | 1 | 16 | 40 | 1.1 |

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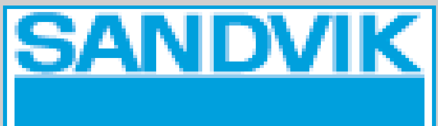

# Use of Sandvik Osprey CE Alloy Wafers

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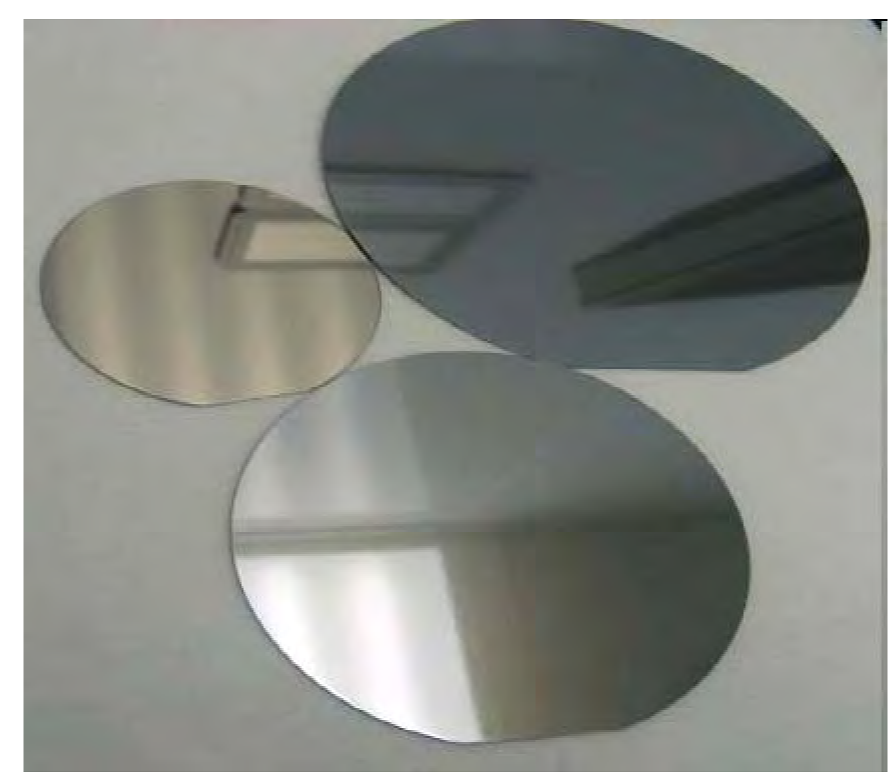
# Current Applications

- The production of CE6 alloy wafers has been driven by demands from two primary markets
  - thermal carrier/substrate for high power, multilayer LEDs
  - high efficiency (up to 41%) photovoltaic cells for PV concentrators



4”, 6” and 8” wafers

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# Typical wafer scale manufacturing technique for vertical structure light emitting diode

Step 1

Sapphire substrate used as substrate for epitaxial growth of LED layers

**US Patent Application US 2006/0268955**

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# Typical wafer scale manufacturing technique for vertical structure light emitting diode

Step 2

Active (light emitting)
semiconductor layers
deposited on wafer

Al-Ga-In-N
eg Al-Ga-In-P

US Patent Application US 2006/0268955

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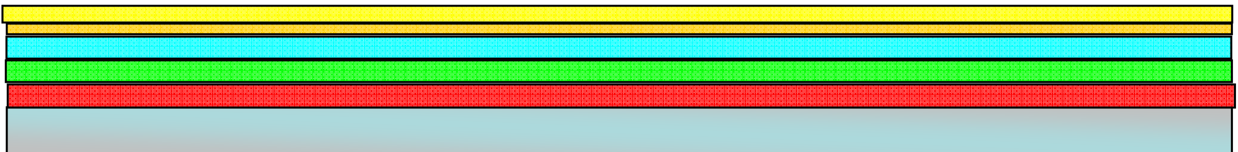
# Typical wafer scale manufacturing technique for vertical structure light emitting diode

Step 3

Deposit metallic
reflective layer (eg Au)

and bonding layer (eg Au-Sn)



US Patent Application US 2006/0268955

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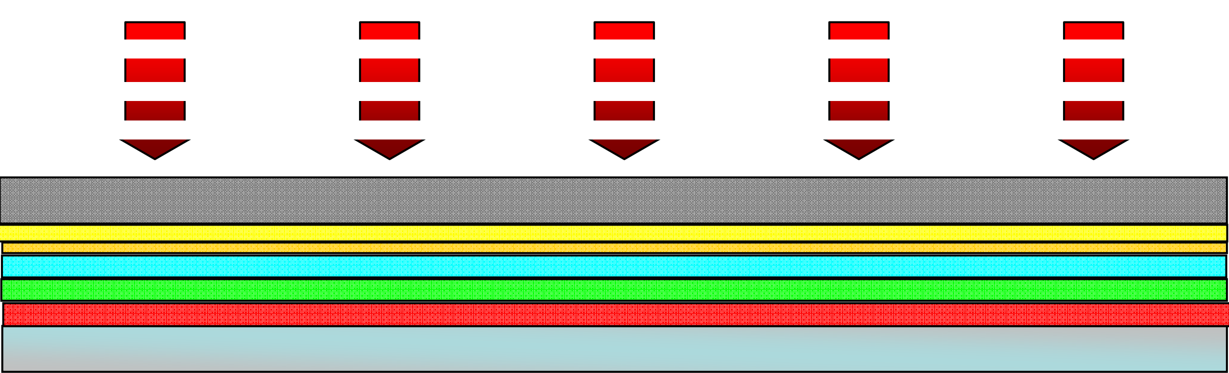
# Typical wafer scale manufacturing technique for vertical structure light emitting diode

Step 4

High temperature soldering of
CE6 wafer to LED device



Virtually flat, stress free structure after bonding
Due to close CTE matching of materials

US Patent Application US 2006/0268955

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# Typical wafer scale manufacturing technique for vertical structure light emitting diode

Step 5

Separate sapphire wafer
using thermal shock

Wafer can be reused

US Patent Application US 2006/0268955

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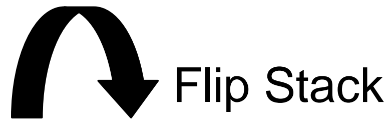
# Typical wafer scale manufacturing technique for vertical structure light emitting diode

Step 6



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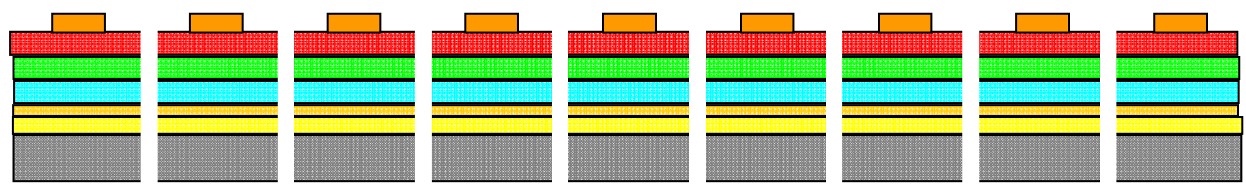
# Typical wafer scale manufacturing technique for vertical structure light emitting diode

Step 7

form n type electrode

and singulate



Silicon as carrier causes mechanical failure (cracking) due to CTE mismatch with active layers

US Patent Application US 2006/0268955

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# Concentrator PV Cells

- Similar wafer scale production methods are have been developed in the PV market where multilayered cells can operate at >40% efficiency

The major driving force in both these application areas is COST reduction
The same is true for high volume RF and Microwave applications

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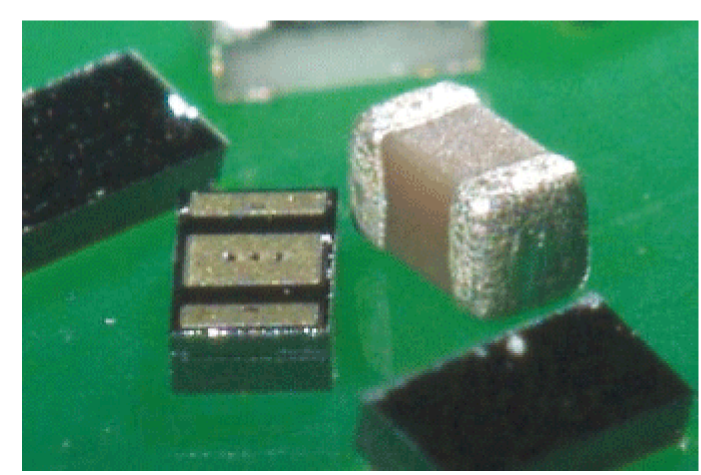
# Example of Wafer Scale RF application

## Wafercap technology

- Avago's Wafercap uses a second 6" GaAs wafer to bond to the device carrying wafer as the substrate.
- This technology has shown that the packaged components can be reduced in size, reduced in cost with an equivalent or enhanced performance.
- The higher thermal conductivity and reduced cost of the CE6 material could possibly improve the cost/performance ratio even more.



1. The WaferCap CSP housing (left) measures just 1.0 x 0.5 x 0.25 mm, occupying the same area as a standard 0402 SMT package, but with a considerable savings in height.

Fujii and Morkner, Microwave Journal, 51,8

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# Example of Wafer Scale RF application

## Wafercap technology

Wafer scale lid

MMIC circuit

Cap wafer

RF MMIC wafer

Bonded wafer

Individually sealed MMICs

Individual MMIC ready for solder assembly

Or for hybrids/ module assembly

2. Packages fabricated with WaferCap CSP technology feature extremely short signal paths for low loss, minimal parasitics, and potential for operation through millimeter-wave frequencies.

Fujii and Morkner, Microwave Journal, 51,8

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# Summary

- CEalloy wafers offer a new, high conductivity alternative wafer material with a controlable CTE in the range 16 to 5ppm/$^{o}$C
- The wafers can be supplied in sizes up to 300mm diameter and down to 0.2mm thick
- The material can be polished and plated like aluminum
- Techniques have been developed for the wafer scale processing of LEDs and PV cells
- Techniques have yet to be developed for wafer scale production of RF and microwave devices using the CEalloy material

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# Thank you for your Interest!

## Sandvik Osprey Ltd.
## Spray Form Group

**http://www.smt.sandvik.com/osprey**
**http://www.cealloywafers.com**

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